**U23EC381 – Electronics and Microprocessors**

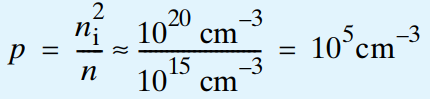
**Answer Key**

**1.** The electrical conductivity of a semiconductor changes appreciably with temperature variations. This is a very important point to keep in mind.

**(i) At absolute zero:** At absolute zero temperature, all the electrons are tightly held by the semiconductor atoms. The inner orbit electrons are bound whereas the valence electrons are engaged in co-valent bonding. At this temperature, the co-valent bonds are very strong and there are no free electrons. Therefore, the semiconductor crystal behaves as a perfect insulator.

**(ii) Above absolute zero.** When the temperature is raised, some of the covalent bonds in the semiconductor break due to the thermal energy supplied. The breaking of bonds sets those electrons free which are engaged in the formation of these bonds. The result is that a few free electrons exist in the semiconductor. These free electrons can constitute a tiny electric current if potential difference is applied across the semiconductor crystal. This shows that the resistance of a semiconductor decreases with the rise in temperature i.e. it has negative temperature coefficient of resistance.

**2.** For each ionized donor, an electron is created. Therefore n = 1015cm–3.



**3.** When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called **pn junction.**

Once pn junction is formed and depletion layer created, the diffusion of free electrons stops. In other words, the depletion region acts as a barrier to the further movement of free electrons across the junction. The positive and negative charges set up an electric field. The electric field is a barrier to the free electrons in the n-region. There exists a potential difference across the depletion layer and is called **barrier potential** (V0).

The typical barrier potential is approximately:

For silicon, V0 = 0.7 V ; For germanium, V0 = 0.3 V.

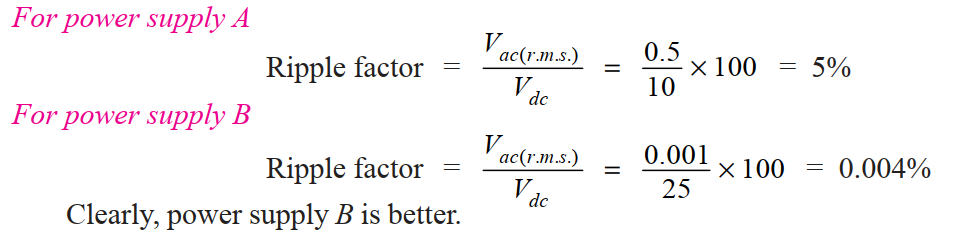
**4.** Two important terms often used with pn junction (i.e. crystal diode) are breakdown voltage and knee voltage. We shall now explain these two terms in detail.

**(i) Breakdown voltage.** It is the minimum reverse voltage at which pn junction breaks down with sudden rise in reverse current.

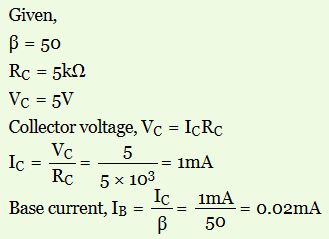
**(ii) Knee voltage.** It is the forward voltage at which the current through the junction starts to increase rapidly.

**5.** Zener diode is a silicon semiconductor with a p-n junction that is specifically designed to work in the reverse biased condition. When forward biased, it behaves like a normal signal diode, but when the reverse voltage is applied to it, the voltage remains constant for a wide range of currents. Due to this feature, it is used as a voltage regulator in d.c. circuit. The primary objective of the [Zener diode](https://byjus.com/physics/zener-diode/) as a voltage regulator is to maintain a constant voltage. Let us say if Zener voltage of 5 V is used then, the voltage becomes constant at 5 V, and it does not change.

**6.** The lower the ripple factor of a power supply, the better it is.

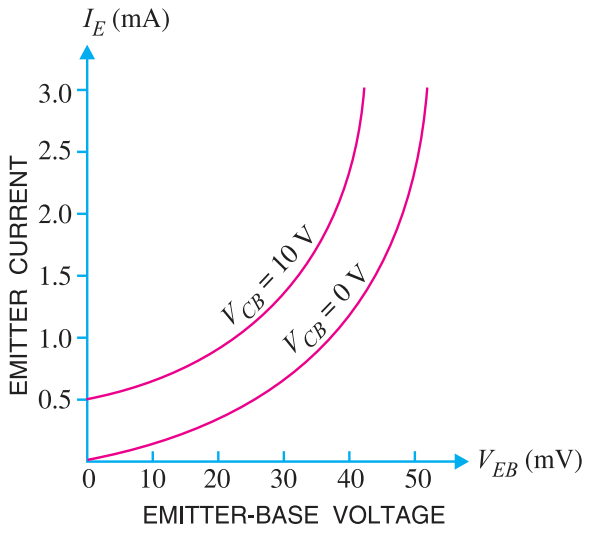


**7.**



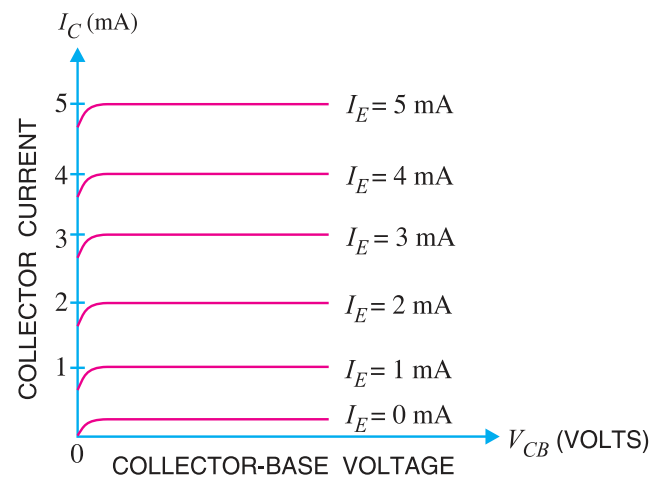
8.

**1. Input characteristic.**



**Inference:** The emitter current *IE* increases rapidly with small increase in emitter-base voltage *VEB*. The emitter current is almost independent of collector-base voltage *VCB*.

**2. Output characteristic.**



**Inference:** The collector current *IC* varies with *VCB* only at very low voltages ( < 1V). When the value of *VCB* is raised above 1 - 2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now *IC* is independent of *VCB* and depends upon *IE* only.

**9.** Given,

IB = 50 µA,

VC = 5 V,

RC = 5 KΩ,

We know that VC = IC \* RC => IC = 5 mA

IE = IB + IC => IE = 5.05 mA

We know that α = = = 0.99

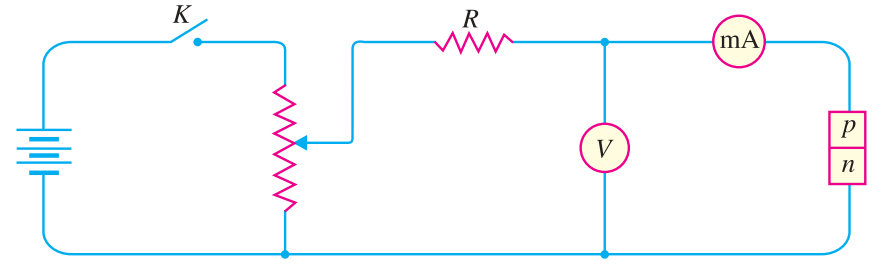
Therefore α = 0.99

**10**.a

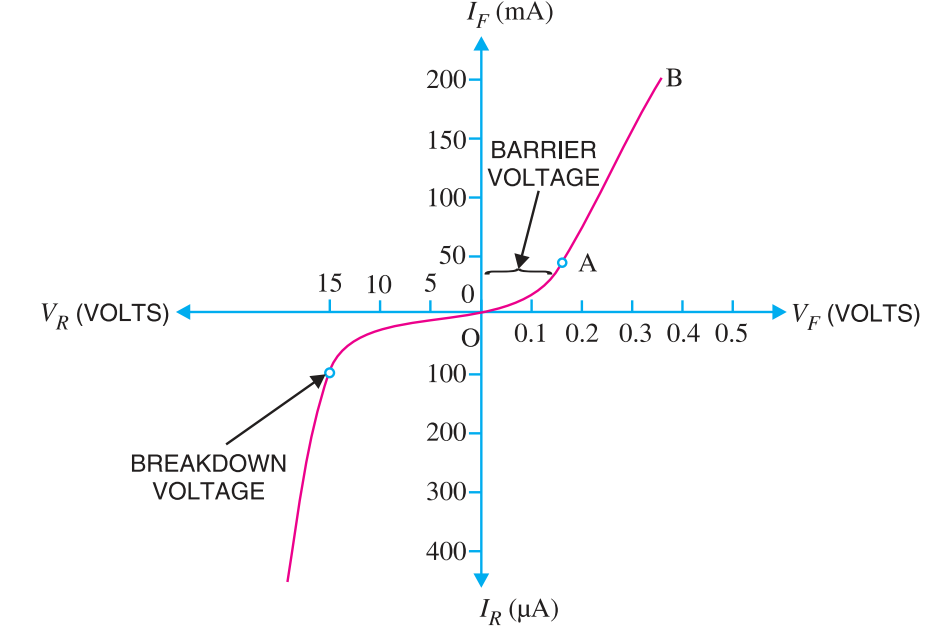
i) **Volt-Ampere Characteristics of *pn* Junction**

Volt-ampere or V-I characteristic of a pn junction (also called a crystal or semiconductor diode) is the curve between voltage across the junction and the circuit current. Usually, voltage is taken along xaxis and current along y-axis. Figure below shows the \*circuit arrangement for determining the V-I

characteristics of a pn junction. The characteristics can be studied under three heads, namely; zero external voltage, forward bias and reverse bias.



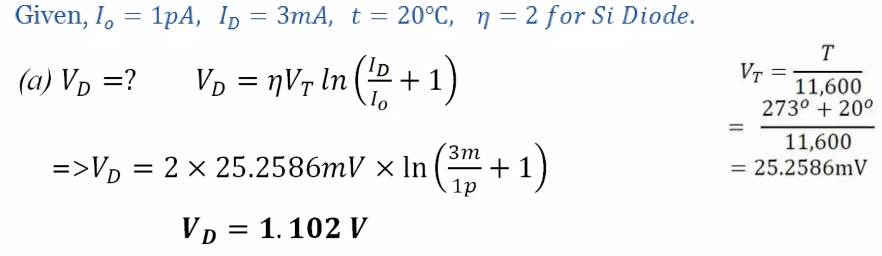
**(i)Zero external voltage.** When the external voltage is zero, *i.e.* circuit is open at *K*, the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point *O* in figure below.

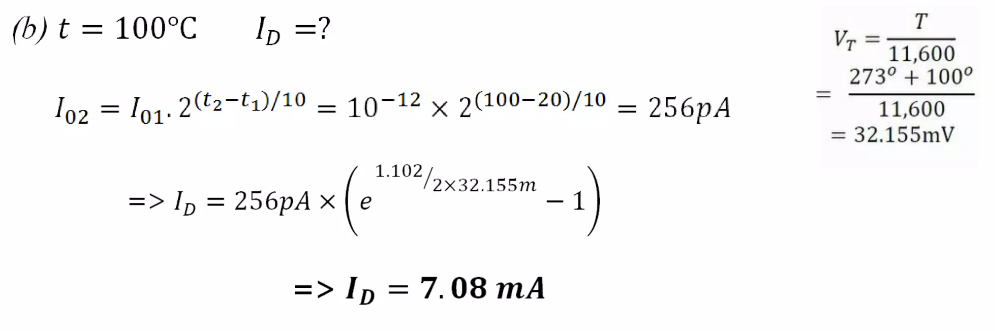


**(ii)Forward bias.** With forward bias to the pn junction i.e. p-type connected to positive terminal and n-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7 V for Si and 0.3 V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage. Thus, arising curve OB is obtained with forward bias as shown in figure above. From the forward characteristic, it is seen that at first (region OA),the current increases very slowly and the curve is non-linear. It is because the external applied voltage is used up in overcoming the potential barrier. However, once the external voltage exceeds the potential barrier voltage, the pn junction behaves like an ordinary conductor. Therefore, the current rises very sharply with increase in external voltage (region AB on the curve). The curve is almost linear.

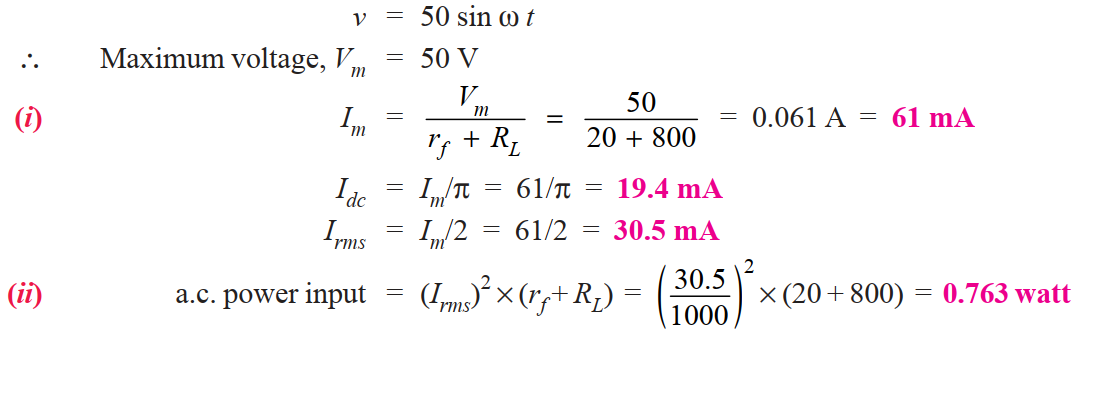
**(iii) Reverse bias.** With reverse bias to the pn junction i.e. p-type connected to negative terminal and n-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit. However, in practice, a very small current (of the order of µA) flows in the circuit with reverse bias as shown in the reverse characteristic. This is called reverse \*saturation current (Is) and is due to the minority carriers. It may be recalled that there are a few free electrons in p-type material and a few holes in n-type material. These undesirable free electrons in p-type and holes in n-type are called minority carriers.

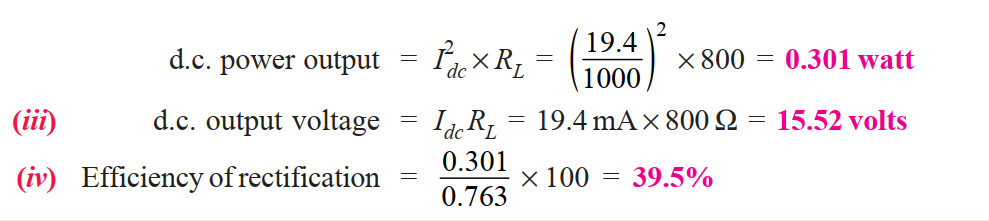
**10**.a

ii) 

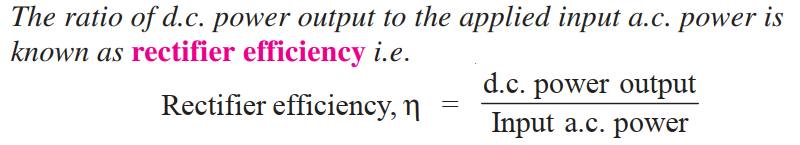


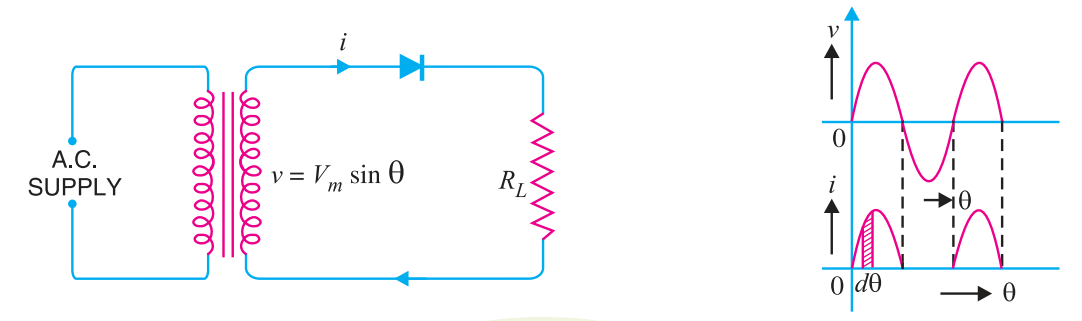
**10**.b

i) 

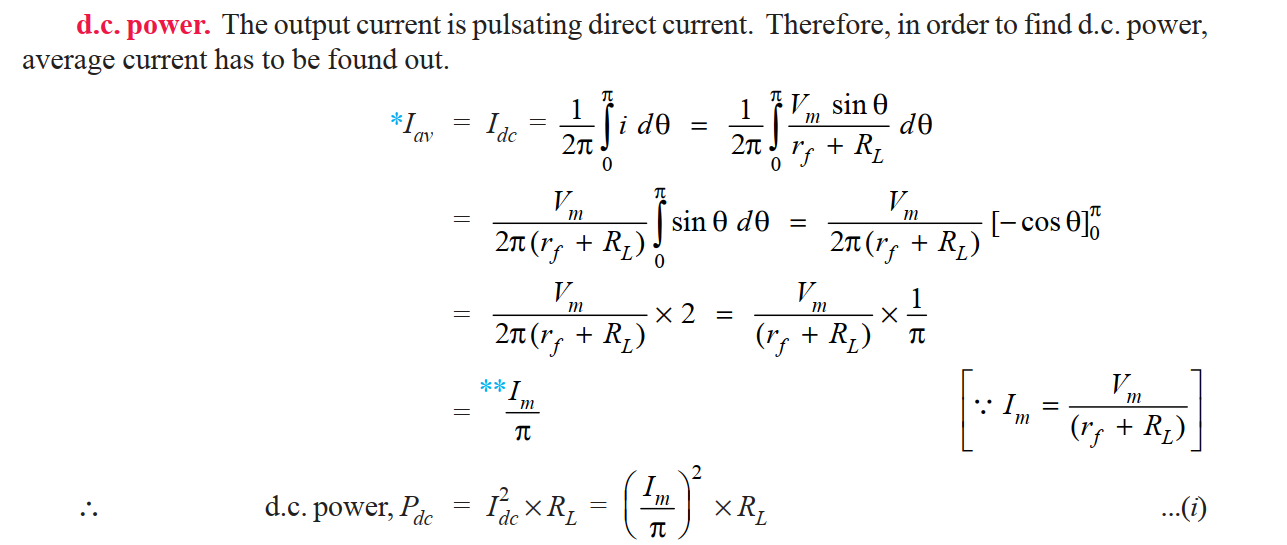


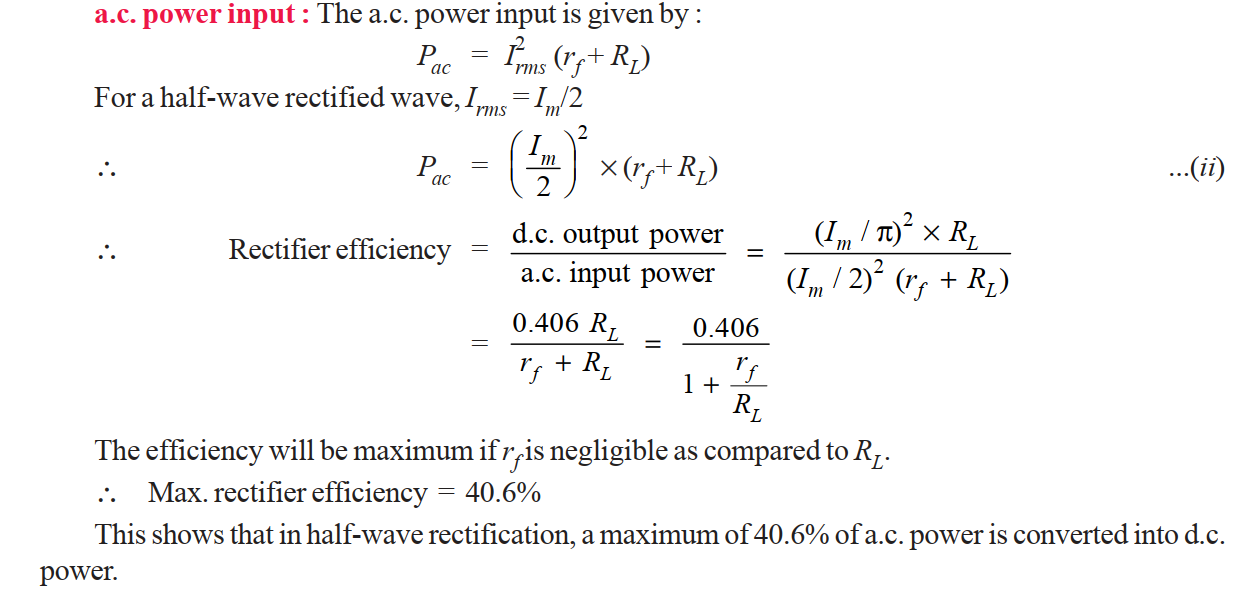
**10**.b

ii) 

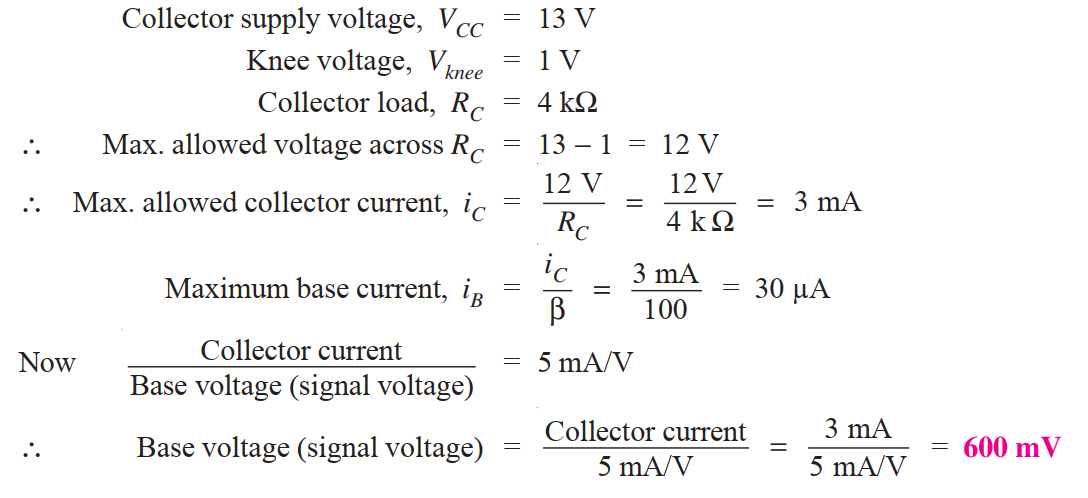


Consider a half-wave rectifier shown in Figure above Let *v* = *Vm* sin θ be the alternating voltage that appears across the secondary winding. Let *rf* and *RL* be the diode resistance and load resistance respectively. The diode conducts during positive half-cycles of a.c. supply while no current conduction takes place during negative half-cycles.

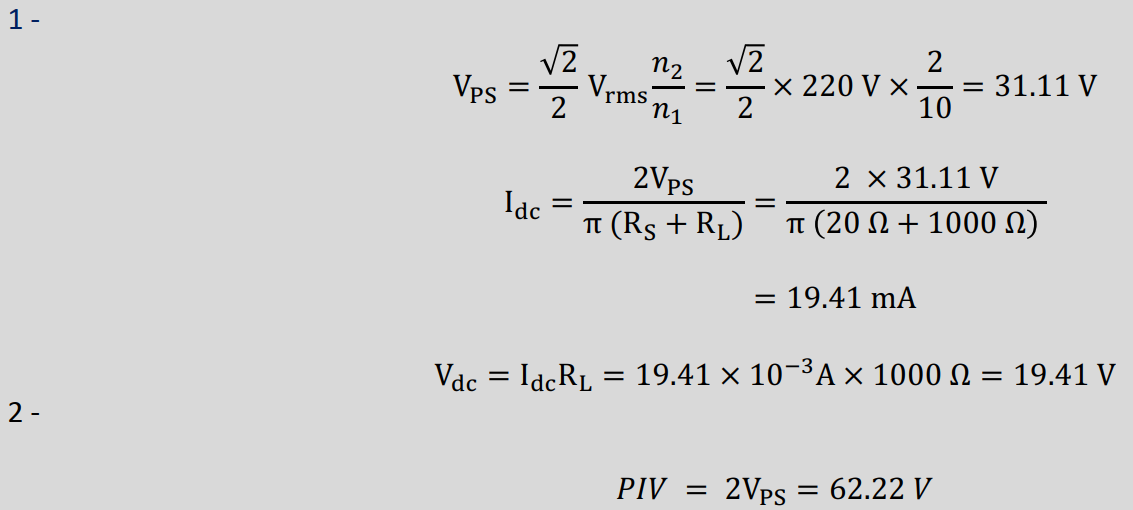


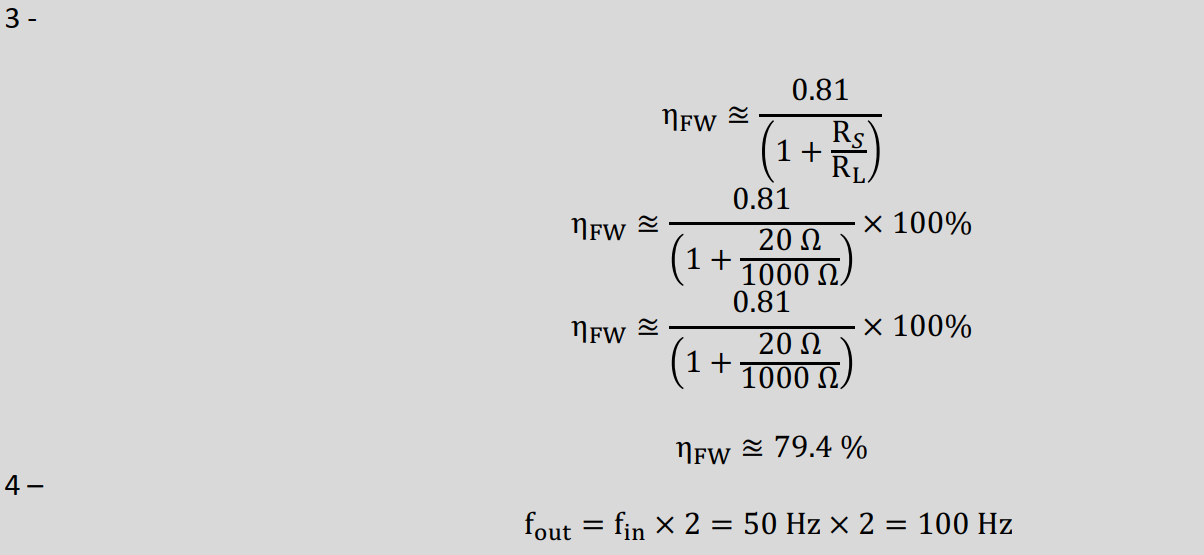


**11**.a

i) 

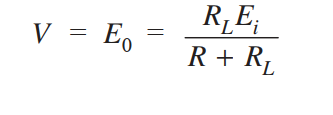
**11**.a

ii) 



**11**.b

i)



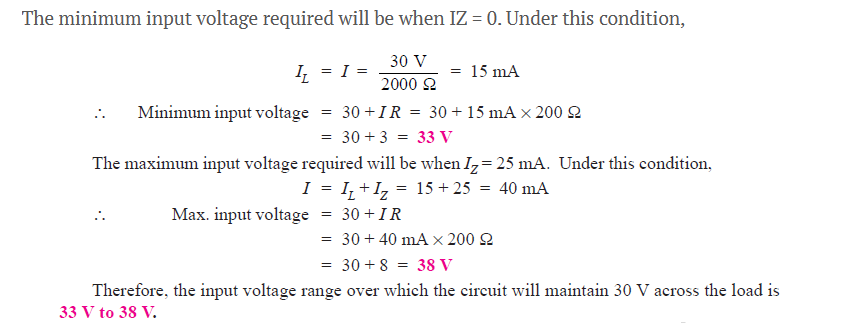
Given that RL = 3 kΩ,

Ei = 14 v,

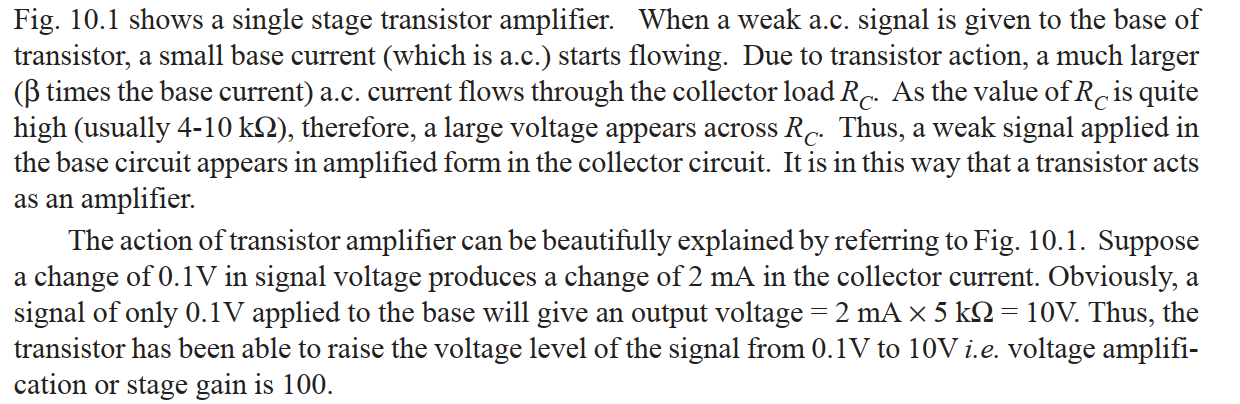
R = 1kΩ

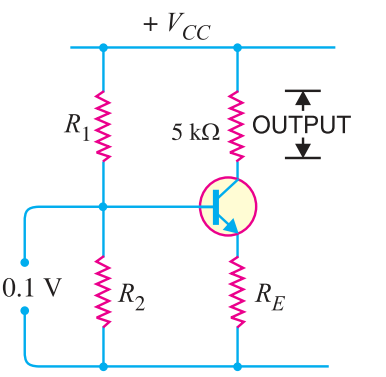
Therefore V = E0 = 10.5 v. And given that VZ = 10 v

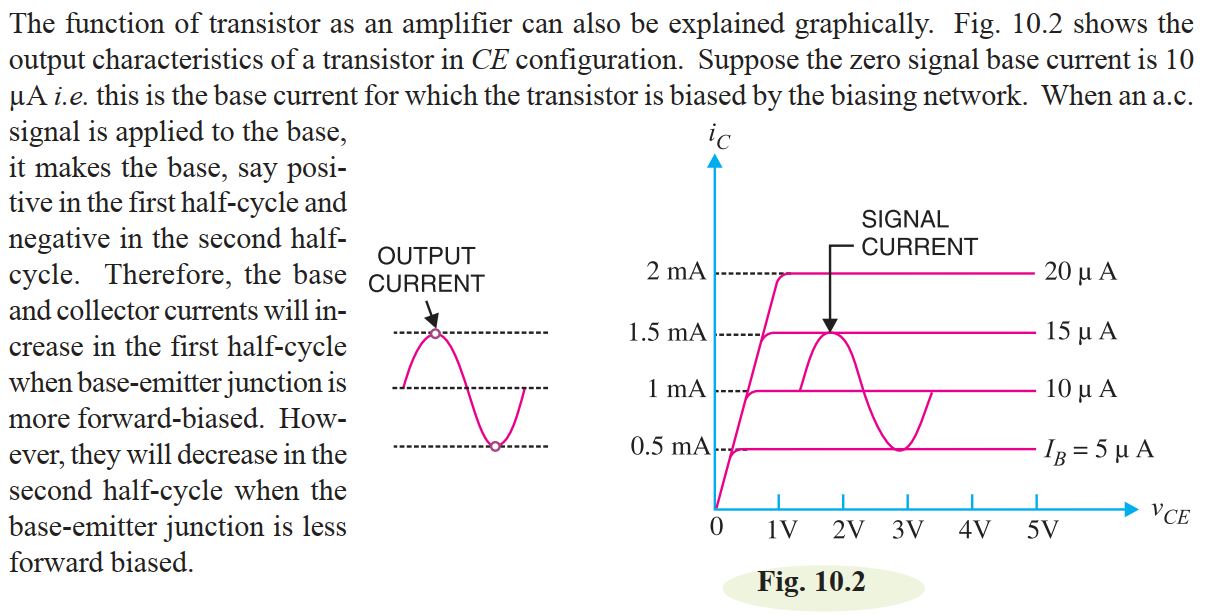
V>VZ => 10.5>10 => the Zener diode is in “on” state.

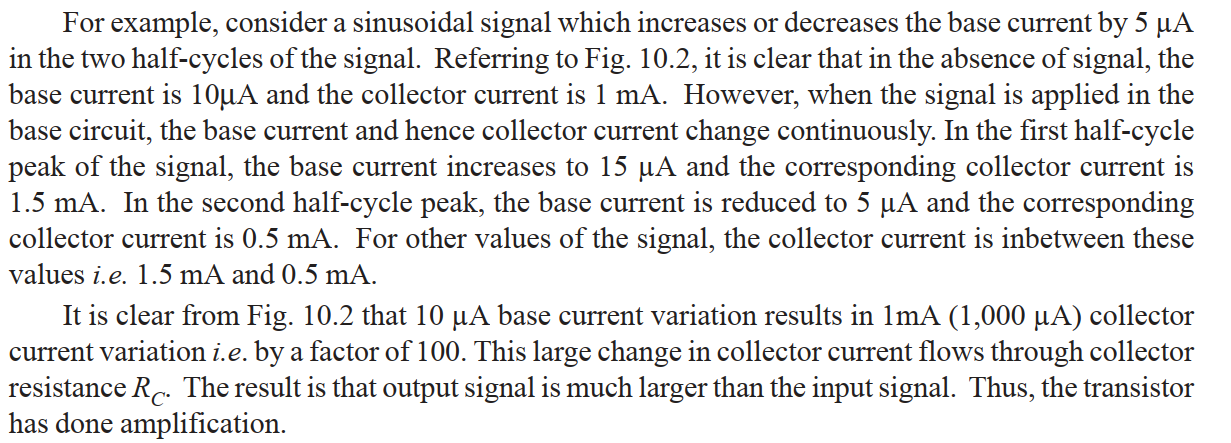
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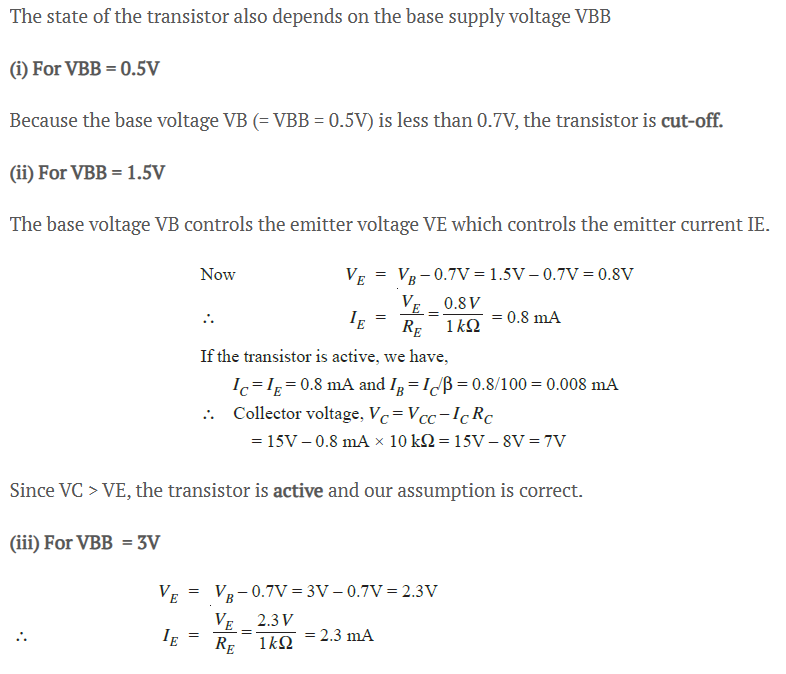
**12**.a

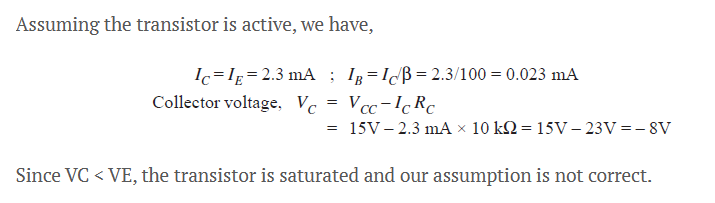
i)







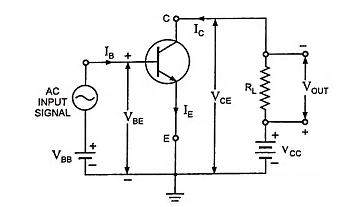
**12**.a ii) 



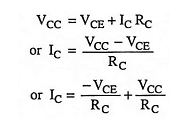
**12**.b

i) The concept of Transistor load line analysis is very important in understanding the working of a transistor. It is defined as the locus of operating point on the output characteristic of the transistor. It is the line on which the operating point moves when ac signal is applied to the transistor.

**DC Load Line:**



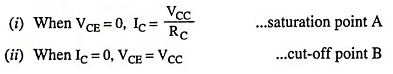
In the circuit shown in figure above, VCC is the supply voltage to collector, RC (or RL) is the collector resistance (or load resistance) and VCE is the collector-to-emitter voltage. Applying Kirchhoff’s second law to the output or collector circuit we have,



This equation is to be plotted on the output characteristic of the transistor, VCE and lC are variables.

Identify this equation as y = mx + c where m = -1/RC as the slope of the line and IC = VCC/RCas intercept of the line on vertical current axis shown in figure below.

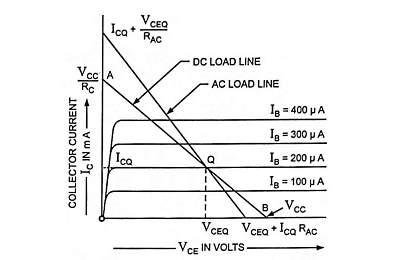
**Consider the following two particular situations:**

[](https://www.eeeguide.com/wp-content/uploads/2022/10/Transistor-Load-Line-Analysis-02.jpg)

By joining these two points A and B, dc load line is obtained. The dc load line represents the dynamic characteristic of the device. The dc load line provides the values of collector current IC and collector-emitter voltage VCE corresponding to zero signal conditions.

### ****Quiescent Point:****

It is a point on the dc load line which represents dc collector-emitter voltage VCE and collector current IC in the absence of ac signal. It is also called the **operating point** because the variations in VCE and IC take place about this point when signal is applied. The best position for this point is midway between cutoff and saturation points where VCE = 1/2 VCC. Point Q is quiescent point marked on the output characteristics shown in figure below.



Selection of the operating point is done as per application for which the device is to be used. For example in case of a small signal amplifier, in which power is conserved, operating point is selected so as to provide lowest quiescent value of lC, while for an amplifier operated to deliver small amount of power, operating point is selected so that available quiescent current is about one-half of the maxi

mum permissible collector current lC.

**12**.bii) 